Please amend the claims as follows.

IN THE CLAIMS:

1. (Currently Amended) A memory circuit comprising at least a non-volatile random access memory, a random access memory, and a memory controller which is connected by a first bus to the non-volatile random access memory and by a second bus to the random access memory, wherein data can be transmitted between said non-volatile random access memory and random access memory via the memory controller, and which memory circuit further comprises a control bus connected to the memory controller, to control the operation of the memory circuit,

wherein the random access memory is useable for running program code substantially simultaneously with the data being transmitted.

2. (Original) The memory circuit according to claim 1, wherein said memory controller comprises means for generating control signals for writing in and reading from the non-volatile random access memory, as well as means for writing in and reading from the random access memory.

3. (Original) The memory circuit according to claim 1, wherein said random access memory comprises a two-port memory.

4. (Original) The memory circuit according to claim 3, wherein the first port of said random access memory is connected to said second bus, and that the second port of said random access memory is connected to a third bus of the memory circuit, to connect the random access memory to an external bus.

5. (Currently Amended) The memory circuit according to claim 1, wherein said non-volatile random access memory comprises or utilizes at least one of the following memory types:

- Flash memory,
- NAND Flash memory,
- NOR Flash memory,
- AND Flash memory,
- EPROM,
- EEPROM,
- fixed disk,
- optical disk.

6. (Original) The memory circuit according to claim 1, wherein said random access memory comprises at least one of the following memory types:

- DRAM,
- SRAM,
- UtRAM.

7. (Currently Amended) A system with a memory circuit comprising at least a non-volatile random access memory, a random access memory, and a memory controller which is connected by a first bus to the non-volatile random access memory and by a second bus to the random access memory, wherein data can be transmitted between said non-volatile random access memory and random access memory via the memory controller, and which memory circuit further comprises a control bus connected to the memory controller, to control the operation of the memory circuit,

wherein the random access memory is useable for running program code substantially simultaneously with the data being transmitted.

8. (Original) The system according to claim 7, wherein said memory controller comprises means for generating control signals for writing in and reading from the non-volatile random access memory, and means for writing in and reading from the random access memory.

9. (Original) The system according to claim 7, wherein said random access memory comprises a two-port memory.

10. (Original) The system according to claim 9, wherein the first port of said random access memory is connected to said second bus, and that the second port of said random access memory is connected to a third bus of the memory circuit, to connect the random access memory to an external bus.

11. (Original) The system according to claim 9, wherein the memory circuit comprises a control bus for the transmission of commands and data between the memory controller and the system.

12. (Currently Amended) The system according to claim 7, wherein said non-volatile random access memory comprises or utilizes at least one of the following memory types:

- Flash memory,
- NAND Flash memory,
- NOR Flash memory,
- AND Flash memory,
- EPROM,
- EEPROM,
- fixed disk,
- optical disk.

13. (Original) The system according to claim 7, wherein said random access memory comprises at least one of the following memory types:

- DRAM,
- SRAM,
- UtRAM.

14. (Currently Amended) An electronic device provided with a memory circuit comprising at least a non-volatile random access memory, a random access memory, and a memory controller which is connected by a first bus to the non-volatile random access memory and by a second bus to the random access memory, wherein data can be transmitted between said non-volatile random access memory and random access memory via the memory controller, and which memory circuit further comprises a control bus connected to the memory controller, to control the operation of the memory circuit,

wherein the random access memory is useable for running program code substantially simultaneously with the data being transmitted.

15. (Original) The electronic device according to claim 14, wherein it comprises a processor for controlling the functions of the electronic device.

16. (Original) The electronic device according to claim 15, wherein said control bus of the memory circuit is arranged to be used for the transmission of commands and data between the memory controller and the processor.

17. (Currently Amended) The electronic device according to claim 14, wherein said non-volatile random access memory comprises or utilizes at least one of the following memory types:

- Flash memory,
- NAND Flash memory,
- NOR Flash memory,
- AND Flash memory,
- EPROM,
- EEPROM,
- fixed disk,
- optical disk.

18. (Original) The electronic device according to claim 14, wherein said random access memory comprises at least one of the following memory types:

- DRAM,
- SRAM,
- UtRAM.

19. (Original) The electronic device according to claim 14, wherein said random access memory comprises a dynamic random access memory, and that the memory controller comprises means for refreshing the dynamic random access memory.

20. (Currently Amended) A method in connection with a memory circuit, in which method at least a non-volatile random access memory, a random access memory, and a memory controller are used in connection with the memory circuit, which is connected by a first bus to the non-volatile random access memory and by a second bus to the random access memory, wherein data is transmitted between said non-volatile random access memory and random access memory via the memory controller, and the operation of the memory circuit is controlled by means of a control bus connected to the memory controller in the memory circuit,

wherein the random access memory is useable for running program code substantially simultaneously with the data being transmitted.